IN THE CLAIMS

Amendments to the Claims:

Cancel claims 11-24 and 29-32.

Listing of claims:

Claims 1-10 and 25-28 (original).

Claims 11-24 ad 29-32 (cancelled).

1. (Original) A vertical semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a gate electrode projecting vertically from said substrate;

at least one semiconducting nanotube extending vertically through said gate electrode between opposite first and second ends;

a gate dielectric electrically insulating said at least one semiconducting nanotube from said gate electrode;

a source electrically coupled with said first end of said at least one semiconducting nanotube; and

a drain electrically coupled with said second end of said at least one semiconducting nanotube.

2. (Original) The semiconductor device structure of claim 1 wherein said source is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

3. (Original) The semiconducting device structure of claim 1 wherein said drain is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

4. (Original) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode.

5. (Original) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode.

6. (Original) The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube is composed of arranged carbon atoms.

7. (Original) The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode.

8. (Original) The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

9. (Original) The semiconducting device structure of claim 1 further comprising:

a plurality of semiconducting nanotubes extending vertically through said gate electrode.

10. (Original) The semiconducting device structure of claim 1 wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

25. (Original) A semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a conductive first plate disposed on said substrate,

at least one nanotube projecting vertically from said first plate and electrically coupled with said first plate;

a conductive second plate positioned vertically above said first plate; and

a dielectric layer electrically isolating said second plate from said first plate and said at least one carbon nanotube.

26. (Original) The semiconductor device structure of claim 25 wherein said at least one nanotube has a conducting molecular structure.

27. (Original) The semiconductor device structure of claim 25 wherein said at least one nanotube has a semiconducting molecular structure.

28. (Original) The semiconducting device structure of claim 25 wherein said dielectric layer defines a coating that encases said at least one nanotube.

ELECTION

Applicants traverse the requirement for restriction and provisionally elect to prosecute claim Group I, consisting of claims 1-10 and 25-28, without traverse.